DS-0 RATE DATAPORT (DS0DP), 628340 AND 628342

GENERAL DESCRIPTION

CONTENTS PAGE

1. GENERAL 1
2. DESCRIPTION 1
3. FUNCTIONAL OPERATION (FIG. 2) 2
GENERAL 2
RECEIVE CIRCUITRY 2
TRANSMIT CIRCUITRY 2
DS0DP CONTROL AND SUBRATE ERROR CORRECTION CIRCUITRY 4
4. OPTIONS 4
5. SPECIAL RESTRICTIONS 4
6. TEST AND MAINTENANCE FEATURES 5
7. TECHNICAL SUMMARY 5
8. REPLACEABLE PARTS 5
9. REFERENCES 5

1. GENERAL

1.01 This Section provides a general description of the ITT D448 DS-0 rate dataport (DS0DP), 628340 (Fig. 1) and 628342, to the functional block diagram level.

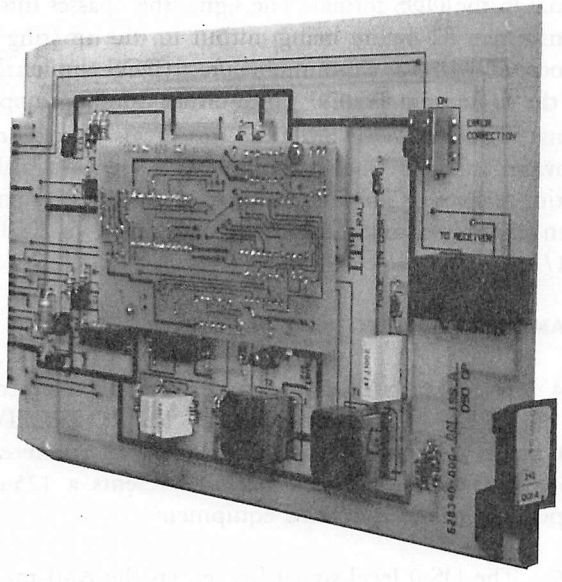

Fig. 1—DS0DP, 628340

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1.02 Whenever this Section is reissued, the reasons for reissue will be listed in this paragraph.

1.03 The DS0DP interfaces the D448 PCM trunk carrier system common equipment with the AT&T Digital Data System (DDS®) network standard format DS-0 level (non-multiplexed customer data at 64.0 kb/s) office signal. This DS-0 level signal may be presented to/from another DS0DP in a nearby D448 multiplex terminal (intra-office trunking applications) or to/from an AT&T DDS subrate multiplexer. The DS0DP will accept either multiplexed (DS-0B) or non-multiplexed (DS-0A) data from the DS-0 level interface.

1.04 The principle functions of the unit are:

(a) In the receive direction, to convert 2.4, 4.8, 9.6, and 56.0 kb/s PCM data from the receive logic unit (RLU) at the 64.0 kb/s rate to DDS-formatted 64.0 kb/s line signals for transmission over a tip/ring pair;

(b) In the transmit direction, to convert the DDS-formatted 64.0 kb/s line signals to 2.4, 4.8, 9.6, or 56.0 kb/s PCM data at the 64.0 kb/s rate for transmission to the transmit logic unit (TLU); and

(c) For 56.0 kb/s error corrected signals, to convert the two channel time slots used for PCM data and error correction at the 64.0 kb/s rate to DDS-formatted 64.0 kb/s line signals for transmission over a tip/ring pair (628342 DS0DP only).

CAUTION: If multiplexed PCM (customer) data at the 64.0 kb/s rate is being used, ensure that the error correction feature is switched off via switch S1 on the 629340 unit, or both switches S1 and S2 on the 628342 unit.

Note: If 2.4, 4.8, 9.6, or non-error corrected 56.0 kb/s data is used, either 628340 or 628342, Groups -001 and -003, may be used. For 56.0 kb/s error corrected data (requiring two adjacent channel time slots), 628342, Groups -004 and -006, are required.

2. DESCRIPTION

2.01 The unit mounts in the D448 multiplex shelf (any channel unit position) in connectors J1A through J24A (for digroup A) or connectors J1B through J24B (for digroup B). Installation procedures are provided in Section ITTR-18-442.

Note 1: The DS0DP mounts in the same channel unit position as its associated office channel unit dataport (OCUDP) on the customer station end of the data service.

Note 2: The 628342, Groups -004 and -006, requires two adjacent (N, N+1) channel unit positions. It physically occupies only one of these positions. To prevent accidental use of the N+1 channel time slot, the blank card unit (BCU), 628099, is installed in the N+1 channel unit slot.

2.02 The 628340 unit is available in Group -001 only. It provides error corrected data at the 64.0 kb/s DDS interface for subrate and non-error corrected 56.0 kb/s data. The 628342 DS0DP is available in the groups listed in Table A.

TABLE A

GROUP NO.	DESCRIPTION
-001 and -003	Provides 64.0 kb/s DDS interface for subrate error-corrected data. 56.0 kb/s error correction not available.
-004 and -006	Provides 64.0 kb/s DDS interface for subrate and 56.0 kb/s error-corrected data.

2.03 The 628340 DS0DP consists of an epoxy-glass printed circuit board (PCB) and associated circuit components. The lower front edge of the PCB is fitted with a handle to facilitate insertion and removal of the unit from the shelf. An identification strip on the handle face indicates the unit mnemonic (DS0DP), part number, and issue letter. The mnemonic, part number, and issue letter are also located on the component side of the PCB.

2.04 The 628342 DS0DP consists of two epoxy-glass PCBs and associated circuit components. The lower front edge of the main PCB is fitted with a handle to facilitate insertion and removal of the unit from the shelf. An identification strip on the handle face indicates the unit mnemonic (DS0DP), part number, and issue letter. The mnemonic, part number, and issue letter are also located on the component side of the main PCB.

2.05 The test access jack (J1) is located on the front edge of the PCB on the 628340 unit and on the front edge of the main PCB on the 628342 unit.

2.06 Printed circuit wiring is etched on both sides of the PCBs. On the 628342-000-001 unit, the PCBs are connected via a connector assembly. The unit inputs and outputs terminate in gold-plated contacts on the rear edge of the PCB (both PCBs on 628342-000-001 and -003 DS0DPs). These contacts mate with a 60-pin contact edge connector on the rear of the multiplex shelf.

3. FUNCTIONAL OPERATION (FIG. 2)

GENERAL

3.01 The following paragraphs describe the operation of the ITT DS0DP.

RECEIVE CIRCUITRY

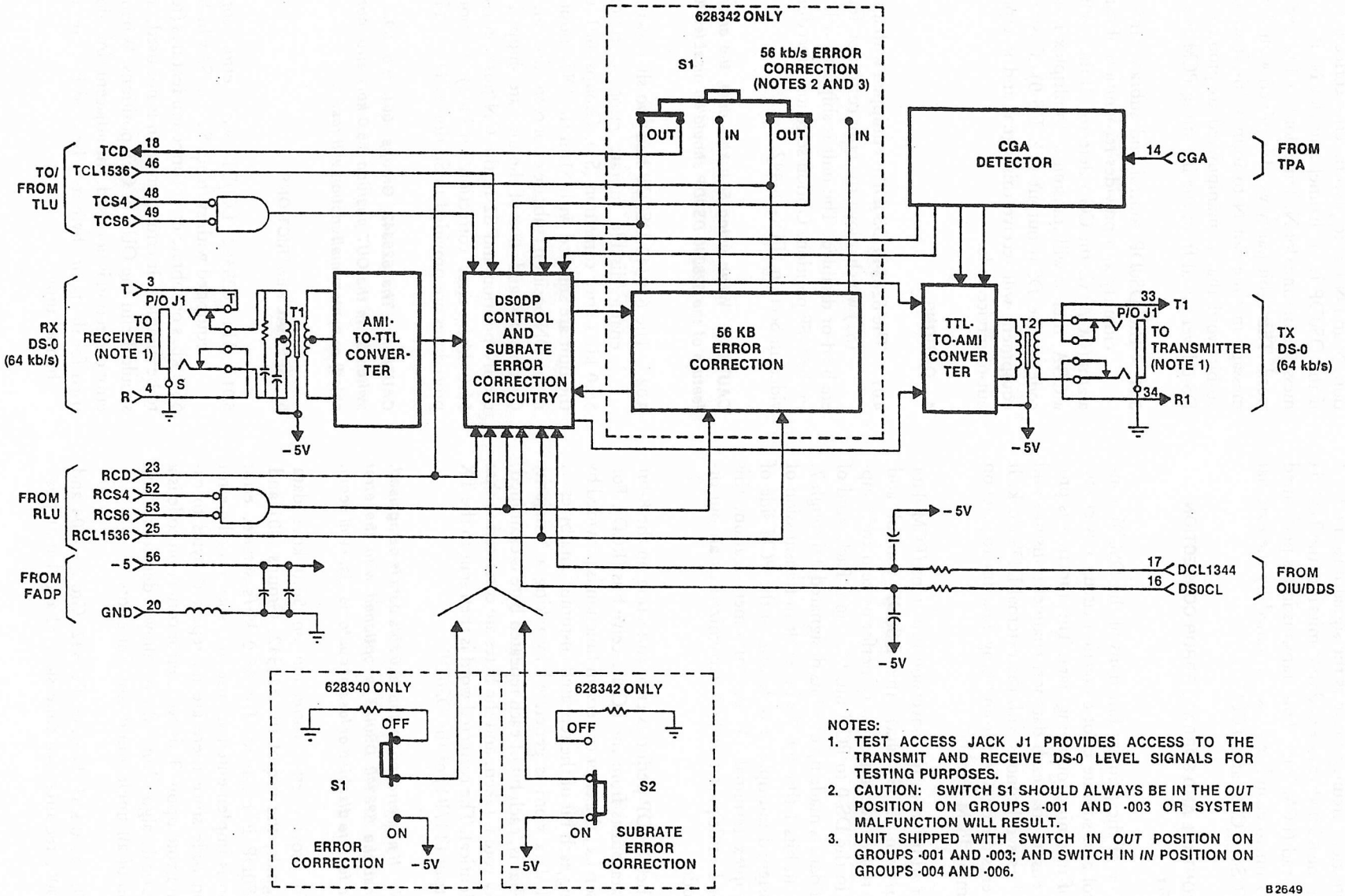
3.02 Customer data signals from the RLU enter the DS0DP via the RCD (PCM bus) lead. These data signals (excluding 56.0 kb/s service) contain repeated bytes of customer data at the original data transmission rate. This byte repetition is performed by the DS0DP and is the method employed for "building up" data signals to the DS-0 interconnect (64.0 kb/s) rate.

3.03 Customer data appearing on RCD is strobed into the DS0DP at 125-microsecond intervals via signals RCS4, RCS6, and RCL1536. The DS0DP control and subrate error correction circuitry (described in Para. 3.06 through 3.11) takes each incoming 8-bit PCM word at the 64.0 kb/s rate, performs error correction, and synchronizes the signal with the incoming DDS clock (DS0CL). It then converts the PCM bit stream to a modified AMI format, and sends it to the DS0DP TTL-to-AMI converter, where the signal is again modified to produce a standard AMI signal in the DDS format. The signal then passes through transformer T2 before being output to the tip/ring pair associated with the DS-0 interconnect (DDS applications) or the co-located DS0DP (intra-office trunking applications). The TO TRANSMITTER test access jack (p/o J1) provides access to the transmitted DS-0 level signal for testing purposes. The DDS-formatted DS-0 level signal is then transmitted to the associated equipment via TX DS-0 (T1/R1).

TRANSMIT CIRCUITRY

3.04 The 64.0 kb/s DDS-formatted signal is received on RX DS-0 (T/R) of the DS0DP. The TO RECEIVER test access jack (p/o J1) provides access to the received DS-0 level signal. Transformer T1 presents a 125-ohm impedance to the associated equipment.

3.05 The DS-0 level signal first enters the AMI-to-TTL converter, where the signal is converted to TTL-compatible logic signals. The DS0DP control and subrate



NOTES:

1. TEST ACCESS JACK J1 PROVIDES ACCESS TO THE TRANSMIT AND RECEIVE DS-0 LEVEL SIGNALS FOR TESTING PURPOSES.
2. CAUTION: SWITCH S1 SHOULD ALWAYS BE IN THE *OUT* POSITION ON GROUPS -001 AND -003 OR SYSTEM MALFUNCTION WILL RESULT.
3. UNIT SHIPPED WITH SWITCH IN *OUT* POSITION ON GROUPS -001 AND -003; AND SWITCH IN *IN* POSITION ON GROUPS -004 AND -006.

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Fig 2—DS0DP, Functional Block Diagram

error correction circuitry converts the signal into the PCM format at the 64.0 kb/s rate and transmits it to the TLU via the TCD lead (PCM bus). This transmission is performed every 125 microseconds and is controlled by the external signals TCS4, TCS6, and TCL1536.

DS0DP CONTROL AND SUBRATE ERROR CORRECTION CIRCUITRY

3.06 One of the primary functions of the DS0DP control and subrate error correction circuitry is elastic storage of incoming/outgoing data. This function is provided to ensure that each dataport channel transmits and receives data synchronous with the external DDS clock. It also prevents the dataport from losing data due to jitter on the incoming PCM signal.

3.07 In addition to its conversion functions (PCM data to/from DDS data), the DS0DP control and subrate error correction circuitry performs zero code suppression in the DS-0 to PCM bus direction. Each word of customer data is made up of 8 bits designated 0 through 7. All zeros in bits 1 through 7 will result in transmission of the unassigned multiplexer code toward the PCM side of the multiplex terminal. At the customer location, this unassigned multiplexer code is recognized as an out-of-service code.

3.08 The DS0DP performs error correction on the 8-bit data bursts from the PCM receive bus (RCD). For subrate service, the error correction function is provided by examining each bit of the repeated customer data bytes. A corrected data word is generated by taking a "majority vote." That is, each bit of each repeated byte is examined, a majority vote is taken, and the bytes are corrected so that all are identical. The corrected word is then sent to the TX DS-0 output (T1/R1) of the DS0DP.

CAUTION: If non-error corrected 56.0 kb/s data is being used, ensure that the 628340 DS0DP is optioned with the error correction feature disabled or loss of customer data will occur.

3.09 To provide error correction on 56.0 kb/s data signals, the use of the 628342, Groups -001 and -003, DS0DP is required. For 56.0 kb/s service, error correction is implemented via use of a special cyclic error correction code since there are no repeated bytes to examine and vote upon. This cyclic error correction code is a mathematical algorithm which allows detection and correction of all single and double bit errors.

3.10 The 56.0 kb/s DS0DP, 628342, Groups -004 and -006, requires two time slots (channel unit positions N and N + 1) to perform error correction. Therefore, if the DS0DP is in channel unit slot N, it transmits data messages in time slot N. Time slot N + 1 is used for a parity word. This 8-bit parity word is joined with the 8-bit data message in time slot N to form a 16-bit word. It is this 16-bit word that is manipulated to produce a corrected DS-0 level signal from the incoming PCM signal.

3.11 The DS0DP control and subrate error correction circuitry also provides recognition of carrier group alarm (CGA) via the CGA detector. If the DS0DP receives a CGA, then it will transmit a "multiplexer out-of-sync" code to the DS-0 output (TX DS-0). Customer station equipment will receive this signal and interpret it as an out-of-service code.

4. OPTIONS

4.01 The 628340 DS0DP is equipped with a slide switch (S1) which allows the error correction feature to be enabled or disabled. The unit is shipped with this switch in the OFF position. Option selection procedures are provided in Section ITTR-18-442.

CAUTION: When using 56.0 kb/s data, the error correction feature of the 628340 DS0DP should be disabled (OFF).

4.02 The 628342 DS0DP had two slide switches which enable/disable subrate error correction (S2) or 56.0 kb/s error correction (S1). Groups -001 and -003 of the unit are shipped with S1 in the OUT position and S2 in the ON position (subrate error correction enabled only). Groups -004 and -006 of the unit are shipped with S1 in the IN position and S2 in the ON position (subrate and 56.0 kb/s error correction enabled). Option selection procedures are provided in Section ITTR-18-442.

CAUTION: The 628342, Groups -001 and -003, must have switch S1 in the OUT position (56.0 kb/s error correction disabled) or system malfunction will result.

5. SPECIAL RESTRICTIONS

5.01 The 628342 DS0DP with error correction is equipped with switches S1 and S2 which allow the 56.0 kb/s or subrate error correction features (respectively) to be disabled. If error correction is not used, the switches should be in the OUT or OFF positions. When 56.0 kb/s error correction is not used, the adjacent time slot normally used for the parity byte may be used by another dataport or channel unit.

6. TEST AND MAINTENANCE FEATURES

6.01 Test access jack (J1) provides access to the transmit and receive DS-0 level signals for testing purposes. Refer to Fig. 1 for the physical location of this feature.

7. TECHNICAL SUMMARY

7.01 A summary of the technical specifications of the units is given in Table B.

TABLE B

ITEM	SPECIFICATION
DC POWER	
Voltage Current Drain	−5.0 ±0.25 Vdc 50 mA nominal (no loop); 150 mA maximum (225 mA maximum for 628342, Group -004)
INPUT IMPEDANCE	125 ohms nominal
OPERATING ENVIRONMENT	
Temperature Humidity Altitude	0° to 55°C To 95% at 40°C (no condensation) To 14,000 ft (4,300 m)
DIMENSIONS	
Height Width 628340 628342 Depth	5.9 in (15.0 cm) 0.8 in (1.9 cm) 1.8 in. (4.6 cm) 9.7 in (24.6 cm)
WEIGHT	0.5 lb (0.22 kg)

8. REPLACEABLE PARTS

8.01 The units contain no field-replaceable parts.

9. REFERENCES

9.01 The engineering drawings noted in Table C were used in the preparation of this Section.

9.02 Related information on the units may be found in Section ITTR-18-442, Dataport Channel Units — Option Selection and Installation.

TABLE C

TYPE	DRAWING NO.
Assembly	628340-000
Schematic	628340-002
Assembly	628342-000
Schematic	628342-002